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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,389	03/12/2004	Amid Hashim	4799-0112P	6042

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EXAMINER	
NGUYEN, HOA CAO	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,389	HASHIM ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *18-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1 pg*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Non patent document (5 pgs)*.

DETAILED ACTION

1. Applicant's election without traverse of Group I, claims 1-17, in the reply filed on 4/12/06 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 11-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Mcclanahan et al. (US 5396397).

Regarding claim 1, as shown in figures 1-5, McClanahan et al. disclose a multilayer printed circuit board (PCB) comprising:

(a) A first section (shaded layers, high dielectric field layers, col.4: 39-41) having a first dielectric constant (high DK, all shaded layers are high DK, col.3: 20-42);

(b) a second section (unshaded layers – basic substrate insulating layers, col.4: 39-41) having a second DK lower than the first DK (col.4: 13-19), and provided above or below the first section (at least figures 3 and 5 show the high dielectric field layers are either sandwiched between the basic substrate insulating layers or in reversed order);

(c) at least one crosstalk compensation element (capacitors, col.5: 23-58; col.4: 44-53; col.5: 17-22) provided in the first section; and

(d) at least one circuit element (all layers have circuit patterns, as shown in the figures, col.4: 44-53) provided in the second section.

Regarding claims 11-12, at least as shown in figure 3, McClanahan et al. disclose the second section (the basic substrate insulating layers) includes:

(a) A first laminate L4 having the second DK (considering middle layer L4 as a laminated layer of a plurality of basic substrate insulating layers, see figures 1-2 and 7-8 for example);

(b) a first prepreg L3 above the first laminate;

(c) a second prepreg L5 below the first laminate; and

(d) all unshaded layers are the second section having a second DK (see claim 1 above).

Regarding claim 13, as clearly shown in figure 3, McClanahan et al. disclose the first section includes:

(a) A third prepreg L2 above the first prepreg;

(b) a first metal layer 35 (a conductive layer) above the third prepreg;

(c) a fourth prepreg L6 below the second prepreg; and

(d) a second metal layer 37 (a conductive layer) below the fourth prepreg.

Regarding claim 14, McClanahan et al. disclose the third and fourth prepregs have the first DK (shaded layers).

Regarding claim 15, at least as shown in figure 3, McClanahan et al. disclose:

(a) The at least one crosstalk compensation element (capacitor for example) is provided at the first and/or second metal layer (col.5: 17-58), and

(b) the at least one circuit element (any circuit element, circuit pattern for example) is provided at a metal sheet (a conductive layer in the basic substrate insulating layers, see figure 5 for example) of the first laminate.

Regarding claim 16, McClanahan et al. disclose the choice of location and **material** for dielectric field control layers (and the basic substrate insulating layers, col. 7: 34-50) is highly dependent on the characteristics of the particular application including, for example, circuit geometry, operating frequencies, power level, and so forth (col.3: 53-62; col.7: 33-50). Therefore, McClanahan et al. anticipate every limitation of the claim including the first DK is in the range of 4.0-5.0, and the second DK is in the range of 2.5-3.5. Furthermore, the discovering the optimum or workable ranges involves only routing skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 17, McClanahan et al. disclose the at least one crosstalk compensation element (passive components, capacitor for example, see col.5: 17-22) includes a plurality of capacitors inherently placed at different compensation stages of the PCB.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 2-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClanahan et al. (US 5396397).

Regarding claims 2-3, as shown in figure 5, McClanahan et al. disclose every limitation as shown in claim 1 above including a first section comprising a plurality of high DK dielectric layers (2 shaded layers shown), but failed to disclose the first section include a first laminate, a first prepreg above the first laminate, and a second prepreg below the first laminate.

In a multilayer circuit board, it is well known in the art that the number of layers having the same dielectric constant is not limited to only two layers depending on a particular application. For example, as shown in figure 7, McClanahan et al. disclose layer L3-L12 are stacked on each other and all having the same dielectric constant; wherein layers L4-L11 are arbitrary selected as a laminate layer, and layer L3 and L12 are arbitrary selected as a first prepreg and a second prepreg formed above and below the laminate layer respectively.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to add more layers to the first section of McClanahan et al. circuit

board such that the first section include a first laminate comprising a plurality of layers, a first prepreg above the first laminate, and a second prepreg below the first laminate in order to increase the capacitance formed by the first laminate.

Regarding claim 4, McClanahan et al. disclose the high dielectric constant field control layers in accordance with the invention can also be printed with passive components, conductive traces, and conductive shields in the same manner as the basic insulating layers included in the multilayer circuit structure (col.5: 17-22). Therefore, McClanahan et al. anticipate every limitation of the claim including the at least one crosstalk compensation element (capacitors, see figure 3, col.23-58) is provided at a metal sheet (a circuit layer or ground or power layer) of the first laminate (choice of location, see claim 3 above).

Regarding claim 5, at least as shown in figure 5, McClanahan et al. disclose the second section (the unshaded layers, the basic substrate insulating layers) includes:

(a) A third prepreg (namely L4) above the first prepreg (considering the top most layer L5 of the high DK layers as the first prepreg);

(b) a first metal layer (above L4 and below L3) above the third prepreg;

(c) a fourth prepreg (namely L7) below the second prepreg (considering the bottom layer L6 of the high DK as the second prepreg); and

(d) a second metal layer (the conductive layer below L7 and above L8) below the fourth prepreg.

Regarding claim 6, at least as shown in figure 5, McClanahan et al. disclose the third and fourth prepregs having the second DK (unshaded layers - the basic substrate insulating layers).

Regarding claim 7, at least as shown in figure 5, McClanahan et al. disclose:

(a) The at least one circuit element (circuit pattern - conductive traces, as shown in the figures) is provided at the first and/or second metal layer, and

(b) the at least one crosstalk compensation element (capacitor) is provided at a metal sheet and/or a dielectric substrate of the first laminate (col.5: 17-22 and col.3: 53-62).

Regarding claim 8, at least as shown in figure 5, McClanahan et al. disclose the second section (the unshaded layers) includes:

(a) A second laminate L1-L4 (a lamination of a plurality of sheets/layers) above the first prepreg (considering the top most layer L5 of the high DK layers as the first prepreg); and

(b) a third laminate L7-L10 (a lamination of a plurality of sheets/layers) below the second prepreg (considering the bottom layer L6 of the high DK as the second prepreg),

(c) the second and third laminates have the second DK (unshaded layers - the basic substrate insulating layers).

Regarding claim 9, at least as shown in figure 5, McClanahan et al. disclose each of the second and third laminates includes a dielectric material substrate (unshaded layers - the basic substrate insulating layers) and a single metal sheet (circuit pattern/conductive traces/ground/power layers) on the substrate.

Regarding claim 10, at least as shown in figure 5, McClanahan et al. disclose:

(a) The at least one circuit element is provided at the single metal sheet of the second and/or third laminate, and

(b) the at least one crosstalk compensation element (capacitors) is provided at a metal sheet and/or a dielectric substrate of the first laminate.

Citation of Relevant Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Nakatani (US 20040040740) disclose an electric element built-in module and method for manufacturing the same.

Okubora et al. (US 20020195270) disclose a high frequency module device and method for its preparation.

Fukuoka et al. (US 6872893) disclose a wiring board provided with passive element and cone shaped bumps.

Mizutani et al. (US 6563058) disclose a multilayered circuit board and method for producing the same.

Rokugawa et al. (US 6441314) disclose a multilayered substrate for semiconductor device.

Tohya et al. (US 6359237) disclose a multi-layer printed board.

Wajima et al. (US 6865090) disclose an outer coating substrate for electronic component and piezoelectric resonant component.

Ninomiya (US 20030024732) discloses a printed circuit board and electronic equipment using the board.

Nakatani et al. (US 6734542) disclose a component built-in module and method for producing the same.

Seri et al. (US 6663946 Multi-layer wiring substrate.

Sugaya et al. (US 6538210) disclose a circuit component built-in module, radio device having the same, and method for producing the same.

Berger et al. (US 6528145) disclose a polymer and ceramic composite electronic substrates.

Fisher et al. (US 20030218870) disclose a low temperature co-fired ceramic with improved shrinkage control.

Horie (US 20030075356) discloses an electronic device and method of manufacturing the same.

Ahn et al. (US 6984886) disclose a system-on-a-chip with multi-layered metallized through-hole interconnection.

Higashi et al. (US 6678144) disclose a capacitor, circuit board with built-in capacitor and method for producing the same.

Iwanami (US 6603668) discloses an interlayer structure with multiple insulative layers with different frequency characteristics.

Novak (US 6215372) disclose a method and apparatus for reducing electrical resonances in power and noise propagation in power distribution circuits employing plane conductors.

Raghu Natarajan and J.P. Dougherty disclose Material Compatibility and Dielectric Properties of Co-Fired High and Low Dielectric Constant Ceramic Package in IEEE, 1997 Electronic Components and Technology Conference.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
5/5/06

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